Data Communications Analyzer 2871

- ☐ **Combined pattern generator and error detector**
- ☐ **Error performance measurements in communications networks from 50 bit/s to 150 kbit/s**
- ☐ **Remote control of instrument facilities via GPIB interface RS–232C (V.24) control interface**
- ☐ **Standard and user-definable CCITT G.821 measurements**
- ☐ **Long-term error performance analysis via histogram display, and 'Autoprint' capability**
- ☐ **8 sets of preserved test conditions**
- ☐ **Interchangeable communications interfaces to support a wide range of signal types**

The 2871 Data Communication Analyzer consists of a pattern generator and error detector combination, plus a powerful processing facility, which is coupled to an extensive range of measurement options.

These elements are combined to form part of a comprehensive error performance test set, which provides for 'out-of-service' and 'in-service' monitoring and testing.

The menu-driven instrument can be manually operated, using the front panel interactive keyboard, or remotely operated via the standard GPIB or RS–232C (V.24) control interfaces. A large (7 inch) CRT screen is used to present a clear indication of both measurement settings and results. A permanent record of the test results can be made available using an external printer.

As a combined pattern generator and error detector, the 2871 simulates a DTE (Data Terminating Equipment). By selecting a suitable internally generated test pattern, and applying it to the network through any of the communications interfaces, a wide range of 'out-of-service' tests can be carried out.

Alternatively, the 2871 is able to implement 'non-intrusive' testing. This 'in-service' test method relies on processing the framing bits of structured live traffic in order to determine the error performance of the communications link. In addition to monitoring the framing bits, other properties of the traffic could be used to carry out the analysis, for example, a test pattern could be added to the traffic and continuously monitored for errors.

2871

Traditionally, the error performance of data connections has been measured over long averaging periods, with the resulting information being presented as a single entity, which is expressed as a ratio of the number of bits received in error to the total number of bits received.

The emphasis today is on determining the distribution of errors by using shorter averaging periods, typically minutes and seconds. By presenting the information in this way more can be revealed about the network performance when carrying different services. For example, randomly distributed errors are disruptive to data services, but below a certain rate have minimal effect on voice transmissions. Conversely, burst errors are less tolerable in telephony and video services, but disrupt data-type transmissions to a smaller extent.

The 2871 has been designed to address the problems that surround the effect bit errors have on digital services.

Along with the normal features contained in measuring instruments of this type, a number of unique measuring facilities are made available to the user.

SPECIAL FEATURES

Graphical display

In this mode, accumulated test pattern or frame alignment bit errors are presented in a graphical form. The vertical axis represents the number of errors, and the horizontal axis a timebase, which is labelled with date and time. The CRT displays the information as a histogram, with a 30 hour or 1 hour time window, each bar of the histogram representing 1 hour or 1 minute respectively. The 1 hour window is selectable from any of the hours in the 30 hour window by operating the front panel cursor control.

In addition to displaying the error occurrences, loss of synchronization and periods when the test has been suspended are indicated on the relevant timebase. A printout of the measurement information is available in a text format, via the GPIB or RS–232C (V.24) control interfaces.

Autoprint

One of the more important aspects of monitoring the network performance or locating system faults is to be able to resolve the time/date and number of occurrences of specified events. This is especially true of those events that occur infrequently.

The 2871 Autoprint facility is able to automatically output information via either GPIB or RS–232C (V.24) control interfaces. The information identifies the event type, the time and date of its occurrence resolved to the nearest second, and the instrument identity number.

This facility is available for the following events, any of which can be chosen to initiate the printout.

a) Start and end of test.
b) Loss and restoration of synchronization (identifies reason for sync loss).
c) Remote loop activation and deactivation.
d) Detection of test pattern error.
e) Detection of envelope alignment bit error.
f) Detection of block error.
g) Change of status bit or X.50 housekeeping bits.
h) Detection of an error-ratio change across two independently selectable BER thresholds in the range 10^3 to 10^8.
i) A cumulative printout of measurement page results at preselectable intervals of 15, 30 mins, 1, 12 or 24 hours or at midnight.
j) A printout of the error distribution page every hour and/or 24 hours/midnight.

Items (a), (b) and (c) are permanently available.

CCITT X.50 Recommendation

The X.50 Recommendation defines the requirements surrounding the multiplexing of synchronous data networks operating at a gross bit rate of 64 kbit/s. The basic multiplexed information is contained in 8-bit envelopes, which are interleaved into a framed structure whose aggregate user data rate is 48 kbit/s. These interleaved 8-bit envelopes appear on the 64 kbit/s bearer at any of four prescribed user data rates set between 0·6 kbit/s and 9·6 kbit/s.

2871 X.50 facilities

In addition to the standard X.50 user data rates, the instrument can also operate with 1·2 or 19·2 kbit rates. Within the 2871 two modes of operation exist which provide an X.50 error rate test facility.

The instrument internally generates the X.50 structured signal with a test pattern inserted into any selected channel at the prescribed bit rate. The remaining channels can carry all ones, all zeros, or a 2^7–1 PRBS signal. The structure's housekeeping bits can be set to either logic state.

Drop and Insert

The instrument is able to receive an externally generated X.50 signal operating at 64 kbit/s, on co-directional, NRZ, or WAL–2 codes. Prior to the re-transmission of the externally applied signal, a test pattern may be inserted into any channel, whilst at the same time dropping the existing signal (Drop and Insert) in that channel.

Loopback and end-to-end tests are available in either mode of operation. Non-intrusive testing is accomplished by monitoring the X.50 structure housekeeping and framing bits.

Preserved conditions

Despite the fact that many measuring instruments available today are multifunction, the average user seldom varies his test set-up parameters from a few well-used routines. In addition to independent front panel operation, the 2871 provides for eight sets of measurement parameters to be selected and stored in non-volatile memory. Each store can be identified by a 10 character label, plus date and time. The stored information can be recalled by the user whenever required. This facility allows the user to rapidly switch from one test routine to another, whilst at the same time requiring the minimum knowledge of the test equipment's operating features.

Power failure—Test Continue functions

During prolonged periods of testing it is feasible that the installation could suffer a mains power failure. In the event that the tester is running unattended, it is important that a record is kept of this occurrence and that on resumption of power, the test routines continue to be carried out. This is especially true for applications involving long-term testing.

In order to enhance the user's confidence in measurement results gained during unattended test periods, these facilities have been made available in the 2871.

CCITT G.821 Recommendation

CCITT G.821 Recommendation supports a method of determining the error performance of a digital line system operating at 64 kbit/s within the concept of an ISDN.

G.821 is based on the recognition that the distribution of errors with time affects different communications services by varying degrees.

The measurement philosophy adopted is to present the error information in two broad categories, one which is relevant to voice and video services, the other to data type services.

The 2871 processes the error information and displays the results in a format which allows the user to assess the system performance based on G.821 parameters.

In addition to assessing the error performance using the standard G.821 measurement parameters, the 2871 provides a separate set of user-definable measurement parameters. This facility will offer extra flexibility to the user as digital networks develop, and modifications to the test definitions occur.

Interchangeable communications interfaces

In today's data communications environment, the equivalent measurement problems can be identified in a number of different networks. Access to the data within the network can be through different communications interfaces. The 2871 recognises this requirement and enables its measurement facilities to be available through an expanding range of inter-changeable interfaces.

The current range includes:

RS–232C (V.24)
V.35
RS–449
X.21
Co-directional
Contradirectional
Binary.

} Available via a rear-mounted panel using 4 mm sockets.

Co-directional, Contradirectional and Binary Interfaces are permanently available on the front panel, or through 4 mm sockets mounted as an interchangeable module on the rear of the instrument.

TRANSMITTER SECTION

SIGNAL CODING

120 ohm balanced

Co-directional
32 kbit/s to 150 kbit/s and includes 64 kbit/s signal to CCITT Rec. G.703.
Contradirectional
32 kbit/s to 150 kbit/s and includes 64 kbit/s signal to CCITT Rec. G.703.
AMI (Alternate Mark Inversion)
AMI 100% signal.
AMI 50% signal.
Pulse amplitude at centre:
Normal ±1 V ±0·05 V into 120 Ω resistive load.
Variable level
Applies to Co-directional, Contradirectional, AMI 50 and 100% signal levels.
Level varies between 0·1 V and 2 V peak in 0·01 V increments.

Binary

TTL/CMOS compatible.
NRZ signal.
Biphase S and M signal.
WAL–2 signal.
Output Circuit: TTL drive with 820 Ω collector load and 150 Ω series resistor.
Output level: Logic "0" < 0·8 V
Logic "1" > 3·5 V

VII Balanced

NRZ signal.
Biphase S and M signal.
WAL–2 signal.

Note: 1) AMI 50% requires a bit rate of 32 times clock. 2) No timing is available with AMI, 50% WAL–2, or Biphase.

TRANSMITTED BIT RATES kbit/s

Internal/external

The following bit rates may be selected using the Internal OR External Clock, the external clock being at the bit rate or at 16 times the bit rate.

0.050	1.000	4.800	25.600
0.075	1.200	6.000	32.000
0.100	1.500	6.400	36.000
0.150	1.600	7.200	38.400
0.200	1.800	8.000	48.000
0.300	2.000	9.600	57.600*
0.400	2.400	12.000	64.000
0.500	3.000	12.800	72.000
0.600	3.200	14.400	76.800
0.750	3.600	16.000	96.000
0.800	4.000	19.200	128.000
0.900		24.000	144.000

External only

Any other bit rate up to 150.000 kbit/s may be selected by application of a bit rate or sixteen times bit rate external clock.
*In particular this allows operation at 56 kbit/s.

CLOCK SOURCE

Dependent upon the selected output signal, the transmitter clock source may be:
a) The internal crystal controlled clock.
b) External TTL—a square wave at the bit rate, sub-multiple of the bit rate or at 16 × the bit rate.
c) External Balanced—either a balanced signal at 2048 kHz or a contradirectional clock signal to CCITT G.703.
d) Receiver Timing—internal connection of a signal derived from received data or timing signals.

Internal Clock Accuracy

Accuracy of the internal crystal controlled clock is ±50 p.p.m.

Timing Signal Output

a) A TTL/CMOS compatible square wave of fundamental frequency equal to the transmitted bit rate of the binary signal. All transitions of the data signal will coincide with transitions from Low to High on the timing signal.
b) For AMI 100%, a balanced square wave at the bit rate. Pulse amplitude = 0·5 V into 120 Ω.

SIGNAL TYPE (STRUCTURES)

a) Unstructured test patterns: The selected test pattern is transmitted as a continuous sequence of data bits.
b) Structured test pattern (6 + 2)—The selected test pattern is divided into a six bit word preceded by an envelope alignment bit (F bit) and followed by a status bit (S bit). The Status bit may be set to either logic state, except during loop testing.
8—Bit Reiteration. The envelope alignment bit alternates between 1 and 0 in successive envelopes. Reiterated envelopes retain the same alignment bit state.
7—Bit Reiteration. The envelope alignment bit alternates between 1 and 0 in each octet at the 64 kbit/s rate, irrespective of the data rate.
Note: Structured data at 6 + 2, changes the bit rate by the ratio 4/3, e.g. an original data rate of 2.4 kbit/s produces a data channel rate of 3.2 kbit/s.

2871

Reiteration
Transmitted bit rate of 64 kbit/s. For channel rates of 12.8 kbit/s and below, the envelopes are reiterated the appropriate number of times to produce the transmitted bit rate of 64 kbit/s.
6 + 2 structured signal data rates may be selected from the following:

0.6 kbit/s	1.2 kbit/s	2.4 kbit/s
4.8 kbit/s	9.6 kbit/s	48 kbit/s

c) Structured test pattern (8 + 2)—12 kbit/s and below. The selected test pattern is divided into an eight bit word, each word is preceded by an envelope alignment bit (A bit) and a status bit (S bit). The status bit may be set to either logic state except during loop testing. The envelope alignment bit alternates between 1 and 0 in successive envelopes. Structured data at 8 + 2 changes the bit rate by the ratio 5/4.
d) CCITT Rec X.50 Division 2 (80 Channel), Division 3 (20 Channel) Structures.
Division 2: Each of the five phases may carry either one 9.6 kbit/s, two 4.8 kbit/s, four 2.4 kbit/s, eight 1.2 kbit/s, or sixteen 0.6 kbit/s data rate signals.
Division 3: Each of the five phases may carry either one 9.6 kbit/s, two 4.8 kbit/s, four 2.4 kbit/s data rate signals.
A data rate of 19.2 kbit/s is also available by combining two selectable 9.6 kbit/s channels.

X.50 OPERATION

The X.50 structure is internally generated.

Generate
The selected test pattern is inserted into a selected channel. All other channels may contain either all zeros, all ones, or a PRBS 2^7-1. The structure's housekeeping bits may be set to either logic state.

Drop and Insert
An externally generated X.50 signal may be applied and the selected test pattern will be inserted into the selected channel. The entire X.50 signal is then retransmitted.
The external X.50 signal may be applied in a co-directional, NRZ or WAL–2 format, but must be at 64 kbit/s.

X.50 External Signal Inputs
TTL compatible input for the application of a 64 kbit/s X.50 structured NRZ or WAL–2 signal.
Balanced Input for the application of a 64 kbit/s X.50 structured co-directional signal to CCITT Rec G.703.
Refer to external clock inputs for electrical characteristics.

Error Injection and Remote Loop Activation
Both facilities are available on the selected channel in both X.50 operating modes.

TEST PATTERNS
The following repetitive test patterns may be selected:
a) All ones (...11111...)
b) All zeros (...00000...)
c) Alternating ones and zeros (...10101...)
d) Pseudo-random binary sequences of:
2^9-1 (511) bits
$2^{11}-1$ (2047) bits
$2^{15}-1$ (32767) bits
$2^{20}-1$ (1048575) bits
$2^{23}-1$ (8388607) bits
e) 16 bit programmable word—Bits 0 to 15 of a 16 bit word may be individually set to either logic state. This is used for unstructured and 8 + 2 working.
f) 12 bit programmable word—Bits 0 to 11 of a 12 bit word may be individually set to either logic state. This is used for 6 + 2 and X.50 working.
g) '50 byte' sequence (or up to 50 bytes) available if unstructured signal type.

ERROR INJECTION
Single errors may be injected manually or automatically into the test patterns or the framing bits of structured data.
Automatic error injection can be preset by multiples of the power of ten within the range 1 in 10^2 to 1 in 10^8.
For structured signals the errors may be distributed across the complete envelope or restricted to the data bits only.
For X.50 structured signals, the errors may be distributed across the total framing bits or restricted to the selected channel's data bits.
For programmable 12 or 16 bit word, errors may be injected manually or automatically into a preselected bit.

REMOTE LOOP ACTIVATION
Prior to any test sequence incorporating a structured signal, custom remote loop activation procedures may be generated.

EXTERNALLY APPLIED JITTER
When controlled from an external clock, the transitions of the digital output signal and timing signal contain jitter components consistent with those of the applied clock signal.

TRIGGER PULSE
To enable the user to view the test pattern on an oscilloscope, a trigger pulse is available for the following signals:
Unstructured and 6 + 2 with no reiteration.
Trigger pulse every other byte except for 'byte messages' when the trigger pulse is once every message.
Reiterated test patterns. There is a trigger pulse every other pattern.
X.50 (internal) structures. There is a trigger pulse once per frame.
8 + 2 structures. There is a trigger pulse every fourth envelope.
Output circuit — TTL compatible.
Pulse width — Normally half unit interval of transmitter bit rate.
Pulse amplitude — 5 V peak nominal.

EXTERNAL CLOCK INPUTS

TTL inputs
TTL compatible input available to a square wave of fundamental frequency equal to the bit rate, sub-multiple of the bit rate or equal to sixteen times bit rate.
Input circuit — Electrically simulates a 5 V CMOS gate with 1K5 resistor to the positive (5 V) rail.

Balanced Input
For the application of a 2·048 MHz signal common to telecomms equipment, or a contradirectional clock signal to CCITT Rec G.703.
Input voltage range: 0·45 V to 2·5 V peak.
Impedance: 120 Ω balanced.

RECEIVER SECTION

Independent operation of the transmitter and receiver sections is available except in the following cases:
a) Transmitted and Received bit rate requires application of an external clock at sixteen times the bit rate.
b) Transmitter timing derives from the received data or timing signals.
c) When operating with plug-in interface.

SIGNAL CODING
Alternative signal code processing is provided, for details refer to Transmitter section.

INPUT CONFIGURATIONS
Balanced, binary and timing signals each have alternative input circuits provided for operation as a direct termination or for termination via a through monitor point.

Inputs 120 Ω balanced
Terminated mode: ± 1 V peak nominal.
Minimum signal level ± 0·55 V peak.
Maximum signal level ± 2 V peak.

Through mode: When a signal from a protected point is received the input sensitivity is in the range of ±31 mV to ±110 mV.

Binary A TTL/CMOS compatible input configured as a Terminated or Protected point input circuit. Each electrically simulates a 5 V CMOS gate with a 1K5 resistor to the positive (5 V) rail when terminated. Input levels logic "0" < 1·5 V, "1" > 3·5 V.

VII balanced Sensitivity: > 300 mV within ±7 V common mode range. Outside this range loss of signal is indicated. Impedance: 3K9 Ω.

RECEIVER BIT RATES KBIT/S Refer to transmitter section.

TIMING SOURCE Dependent upon the selected input signal, the source for receiver timing may be:
a) Received signal — e.g. co-directional, WAL-2, Biphase.
b) External — receiver synchronizes to an externally applied binary square wave.
c) External clock — receiver timing derives from the external sixteen times bit rate clock signal applied to the transmitter.
d) Contra timing (bal EXT CLK input)
e) External Balanced—receiver synchronises to an externally applied balanced square wave.

Receiver Timing Input A TTL/CMOS compatible terminated or protected point input circuit accepts a square wave equal to the bit rate of the received signal. The timing signal transitions from high to low state coincide with the centre of each binary signal data bit.

SIGNAL TYPES The receiver may be set to receive any one of the signal types described in the transmitter section.

TEST PATTERNS The receiver may be set to synchronize to, and detect errors in, any test pattern listed in the transmitter section.

ERROR DETECTION The received signal is compared with an internally generated reference pattern to determine bit errors.
For structured test patterns, the receiver may be set to detect bit errors in the envelope data bits, or alignment bits only.
In reiterated patterns the first envelope only of each frame is examined.
In X.50 structures the total framing bits are monitored and if applicable the groups of six data bits of a selected channel.

INPUT JITTER The receiver will correctly indicate the presence of an error-free input signal when the 64 kbit/s digital signal and timing signal have single sinusoidal jitter components not exceeding the values shown in the table below:

Jitter frequency (Sinusoidal rate of change)	Maximum permitted peak to peak jitter amplitude
20 to 2400 Hz	3·2 µs (0·2 UI)
2·4 to 18 kHz	Reducing from 3·2 µs to 800 ns at 13·8 dB/decade with increase in frequency.
18 kHz to 100 kHz	< 800 ns (< 0·05 UI)

MEASUREMENTS Bit error rates and error performance characteristics of a data connection can be determined using received:
Test pattern bits:
Alignment bits of structured signals.
The receiver takes measurements simultaneously of all test pattern and alignment bit parameters together with one other auxiliary measurement.

Error ratio The error ratio is in the range from 1 in 10^{10} and is expressed in the form M × 10^{-n} where M is an integer number in the range 1 to 9. The method for determining the error ratio of structured signals using the alignment bits only, is based upon the assumption that errors are distributed in a random manner throughout the received digital signal. The probability which follows a Poisson distribution of a given error ratio value being displayed or (having been displayed) up-dated to another value within a stated time period is as shown in Table 2.

TABLE 2

Time periods for display of envelope alignment bit error ratio

Received Bit Rate	Indicated Error Ratio	Average Error Ratio In Rec.	Probability (%) of indicated Error Ratio being displayed or (having been displayed) being updated to another value within the time period.		
			Displayed	Updated	Time Period
6·4 kbit/s	1 in 10^2	1 in 10^2 9 in 10^3 1 in 10^3	54·70% 43·11% 0	4·24% 7·19% 99·09%	1·000s
	9 in 10^3	9 in 10^3 8 in 10^3 9 in 10^4	54·70% 41·77% 0	4·24% 7·62% 99·09%	1·111s
	8 in 10^3	8 in 10^3 7 in 10^3 8 in 10^4	54·70% 40·13% 0	4·24% 8·18% 99·09%	1·250s
	7 in 10^3	7 in 10^3 6 in 10^3 7 in 10^4	54·70% 38·04% 0	4·24% 8·94% 99·09%	1·429s
	6 in 10^3	6 in 10^3 5 in 10^3 6 in 10^4	54·70% 35·22% 0	4·24% 10·07% 99·09%	1·667s
	5 in 10^3	5 in 10^3 4 in 10^3 5 in 10^4	54·70% 31·27% 0	4·24% 11·89% 99·09%	2·000s
	4 in 10^3	4 in 10^3 3 in 10^3 4 in 10^4	54·70% 25·60% 0	4·24% 15·12% 99·09%	2·500s
	3 in 10^3	3 in 10^3 2 in 10^3 3 in 10^4	54·70% 17·00% 0	4·24% 22·17% 99·09%	3·333s
	2 in 10^3	2 in 10^3 1 in 10^3 2 in 10^4	54·70% 5·11% 0	4·24% 43·35% 99·09%	5·000s
	1 in 10^3	1 in 10^3 9 in 10^4 1 in 10^4	54·70% 43·11% 0	4·24% 7·19% 99·09%	10·000s

Test pattern blocks The received signal may be divided into blocks of length:
2^8 to 2^{16} in powers of 2.
10^2 to 10^4 in powers of 10.
The measured parameters are displayed as a block error ratio.

Error-free time Four error-free time measurements are available, only one of which may be selected at any one time.
a) Synchronized percentage error-free seconds.
b) Unsynchronized percentage error-free seconds.
c) Unsynchronized percentage error-free deciseconds.
d) Mean time between errors.
Measurement resolution of error-free time 0·01%

Synchronized error-free time: Error-free seconds are determined by counting the number of times that a one second timer resets from one second to zero. The occurrence of each error bit resets the timer to zero without the reset event being counted.
Unsynchronized error-free time: Error-free seconds (deciseconds) are determined by counting the number of seconds (deciseconds) since commencement of the test during which no error bits have occurred.
Mean time between errors:
MTBE = Elapsed time/Number of error bits.

CCITT G.821 Error performance

The following measurement parameters are based on bit error analysis of a received 64 kbit/s test pattern. To fulfil the overall performance objective the individual parameters are measured and displayed concurrently. The maximum test duration is approximately 180 days.
available time — displays hours-minutes-seconds
unavailable time — displays hours-minutes-seconds
% unavailable time
% minutes with error ratio > 1 in 10^6 are degraded minutes
% seconds with error ratio > 1 in 10^3 are severely errored seconds
% error free seconds

Break measurement

Break measurements qualified as 10 consecutive seconds with a BER > 1 in 10^3. In addition to the standard G.821 parameters, the following information is also displayed:
Error ratio (EXCL SES)
Breaks today
Number of days
% break free days
% days with 1 break
% days with 2 or more breaks

User definable (G.821)

Modifications of the standard G.821 parameters can be made by the user. The use of this facility is not restricted to 64 kbit/s operation and is made available in order to accommodate special measurement requirements.
Available time — displays hours-minutes-seconds
Unavailable time — displays hours-minutes-seconds

Definable parameters

Unavailable time, qualified by selecting 5, 10 or 20 s at BER > 1 in 10^2, 10^3, 10^4, 10^5.
% intervals (minutes) may be set to 10 min or 1 min with error ratio > 1 in 10^x where x may be 5, 6, 7.
% intervals (seconds) may be set to 10 s or 1 s with error ratio > 1 in 10^y where y may be 2, 3, 4 or 5.

HISTOGRAM

During test pattern, alignment bit, G.821 or error-free time measurements, error occurrences are accumulated and are available for display as a histogram of errors. The histogram pages consist of a 30 hour time window, labelled with date and time, and a measurement resolution of 1 hour, or 1 hour time window resolved to 1 minute. The 1 hour page can be selected from any of the hours on the 30 hour page.

MEASUREMENT INHIBIT

All measurements are inhibited and totalisation halted upon occurrence of the following conditions:
a) Loss of received digital signal.
b) Loss of received timing signal (if appropriate).
c) Loss of synchronization.
d) Manually suspended.

TEST DURATION

The duration of the test in terms either of test pattern or alignment bits may be preset in powers of ten over the range 10^4 to 10^{10} bits. The test duration in terms of time may be preset in the range 1 minute to 24 hours. The test may also be set to indefinite duration and manually terminated using the stop key. In this mode the measurement will terminate when the total received bits equal 10^{12}.

BIT RATE TIMING MEASUREMENT

The actual bit rate of the received data may be measured at the beginning of each test routine.

REAL-TIME CLOCK

Displays the date and time on the CRT screen.
Resolution: 1 second.
Accuracy: ± 1 minute/week.

STORAGE FACILITIES

A variety of information may be stored in non-volatile memory.

Last operation

The instrument retains the transmitter, receiver, measurement definition, autoprint parameters at switch-off. These are reinstated when the instrument is turned on.

Preserved conditions

Eight sets of transmitter/receiver/measurement parameters may be selected from non-volatile storage.

Password facilities

The following facilities may be accessed via a four-digit password:
a) Display disable/re-enable — inhibits unauthorised use of the instrument during test periods.
b) Real time clock — date and time amendment.
c) Servicing information — operational hours date last calibrated.
d) Servicing facilities — screen test diagnostics.

AUXILIARY FACILITY

Printer

A 24 or 80 column printer may be connected to the GPIB socket, or the RS-232C (V.24) remote control interface socket on the rear panel.
Printer facilities are manually or remotely accessed via either interface.
When initiating via the RS-232C (V.24) control interface, a hardware or software handshake is required.

POWER FAIL TEST CONTINUE

If mains power is lost during a test, the test is resumed when the power returns. Indications of the power fail are given on the histogram and the autoprint output.

'HELP'

A comprehensive set of HELP pages is available which support both the instrument operation and set-up routines.

GPIB interface

All controls except the supply switch are remotely programmable. Complies with the following subsets as defined in IEEE 488-1978, IEC 625-1 1979 and BS6146: SH1, AH1, T5, L4, SR1, RL1, DC1, PP0, DT0, E2, C0.
For printing to an addressable GPIB printer under local control also C1, C2, C3 and C28.

RS-232C (V.24) control interface

All controls except the supply switch are remotely programmable. All transfers wherever possible use the same mnemonics etc. as the GPIB interface. Control codes are used as GPIB command substitutes: for example SOH & EOT are used as the connect and disconnect (GTL) characters respectively.

Type:	Asynchronous; DTE; Full or half duplex.
Bit rates:	110, 300, 600, 1200, 2400 & 9600.
Code:	ASCII or EBCDIC. Odd, even, mark, space or no parity. 2 Tx stop bits, 1 Rx stop bit.

Handshake:	Full duplex: with or without hardware and/or software handshake. Hardware handshake uses DTR RTS CTS CD DSR. Software handshake uses XON and XOFF. Half duplex: uses DTR RTS CTS CD DSR with STX and ETX as the turnaround character.
Lines used:	Tx data — Rx data RTS — CTS DTR — DSR CD
Connector:	25 way D-type (female) — ISO 2110.
Electrical:	To RS-232C (V.28).
Monitor video	Composite video signal 1 volt nominal peak/peak. 625 lines/50 Hz non-interlaced. 288 video information lines. Output impedance 75 Ω.
DC output	7 pin DIN socket. + 12 V nominal. Expressly provided for optional line printer.

RS-232C (V.24) COMMUNICATIONS INTERFACE

Operating Modes	Full duplex Half duplex — Incorporates end-to-end testing with automatic turn round.
Simulates	DTE (Data Terminating Equipment).
Timing	Synchronous Rx Timing — Pin 17 Tx Timing — Pin 15 Pin 24 (internally generated) Asynchronous timing derived from 2871.
Bit rates	Synchronous/asynchronous — bit/s 50, 75, 100, 110, 134·5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, 19200 19·2 kbit/s is Full Duplex only. The instrument will work synchronously for all bit rates between 50 bit/s to 20 kbit/s. Note. Asynchronous: Transmitter bit rate for 110, and 134·5 bit/s (selected and displayed) will be 112·5 and 136·36 bit/s respectively.
Codes	ASCII — 7 bit plus parity asynchronous, 8 bit synchronous. EBCDIC — 8 bit.
Parity	Odd, even, mark, space, none.
Stop bits	Selectable 1 to 8 (8 consecutive stop bits are inserted every 96 characters).
Electrical	RS-232C (V.28) recommendations
Connector	25 way D-type female/ISO2110.

OPERATING RANGE

Conditions of storage	Temperature: 0 to 55°C. Temperature: − 40 to + 70°C. Humidity: Up to 90% relative humidity (non-condensing). Altitude: Up to 2500m (pressurized freight at 27 kPa differential i.e. 3·9 lbf/in^2).
POWER REQUIREMENT	AC voltage range: switchable voltage ranges 105V, 120V, 210V, 240V ± 10%. Frequency: 45 to 65Hz. Consumption: 120 VA.

DIMENSIONS AND WEIGHT

Height:	Width:	Depth:	Weight:
197 mm 7·75 in	345 mm 13·06 in	470 mm 18·04 in (no cover) 530 mm 20·08 in (with storage cover)	14·5 kg 32 lb

ACCESSORIES

When ordering please quote eight digit code numbers

Ordering numbers	
	Supplied Accessories
52871-9002	Socket Assy Side Entry 2·5 lg 52871-900Z 43129·003W. Cover Stowage 41690-485R. Operating Manual H52871-900Z Vol 1 46881-623L. Interface RS-232C (V.24/V.28) 46883-825H.
	Optional Accessories
43129-189U	GPIB Lead Assembly.
46881-365R	GPIB Manual (H54811-010P).
46883-408K	IEEE/IEC Adapter Block.
54127-304C	Rack Mounting Kit.
46881-624J	Service Manual H52871-900Z Vol 2.
44828-894N	Extender Board Kit.
46883-757U	Interface RS-449.
46883-758Y	Interface X.21.
46883-759N	Interface V.35.
46883-760U	Interface Siemens.
46883-852R	RS-232C (V.24) Adapter, Null Modem Female to Female.
46883-874W	Lead, RS-232C (V.24) DTE to DCE Male to Male.
43126-012S	Signal Lead BNC-BNC.
46662-096C	Carrying Case.
54211-001D	Printer.
46883-877P	Printer Accessories Kit (paper and ribbon).
46883-808D	Lead RS-449 Male to Male DTE to DCE.
46883-809T	Lead V.35 Male to Male DTE to DCE.
46883-810W	Lead X.21 Male to Male DTE to DCE.
46883-805V	Presdat Lead Kit.
46883-872V	Signal Lead (RTG 16).
46883-873S	Signal Lead (RTG 16) Male to Male.